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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/824,569	04/13/2004	Todd Kaplan	B-5327NP 621691-8	6558

7590 01/11/2005

Richard P. Berg, ESQ.
c/o LADAS & PARRY
Suite 2100
5670 Wilshire Boulevard
Los Angeles, CA 90036-5679

EXAMINER	
NGUYEN, LINH V	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 01/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/824,569	KAPLAN, TODD	
	Examiner	Art Unit	
	Linh V Nguyen	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-69* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *42-67* is/are allowed.

6)☒ Claim(s) *1,3,18,19,34-36,41-44 and 68* is/are rejected.

7)☒ Claim(s) *2,4-17,20-33,37-40* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/14/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application No. 10/912,627 filed on 08/05/200. Claims 1 – 20 are pending on this application

Information Disclosure Statement

2. The IDS filed on 01/14/04 has been considered.

Specification

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

4. Claims 37 and 69 are objected to because of the following informalities:

Regarding claim 37, on line 1 of the claim, "claim 34" needs to change to - - claim 36 - -, because claim 34 does not provide proper antecedent basis for "the delta-sigma modulator". While claim 36 is providing proper antecedent basis for "the delta-sigma modulator".

Regarding claim 69, on line 6 of the claim, "second DAC input" needs to change to - - first DAC output - -.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1, 3, 18, 19, 34 - 36, 41 - 43, and 68 are rejected under 35 U.S.C. 102(b) as being anticipated by Adams et al. U.S. Patent No. 5,404,142.

Regarding claim 1, Fig. 6 [20] of Adams et al. discloses switching arrangement (22, 24; Col. 4 lines 58 – 62) comprising: a digital input comprising a first digital input portion (A) and a second digital input portion (B); a digital output (Output of 20) comprising a first digital output portion (Out A) and second digital output portion (Out B); a switching element (22, 24) between the digital input (A, B) and the digital output (Out A, Out B), the switching element having a first condition (Col. 4 line 68 – Col. 5 line 2; disclosing "Low" condition of control signal 26) allowing the first digital output portion (Out A) to correspond to the first digital input portion (A) and the second digital output portion (Out B) to correspond to the second digital input portion (B) (Col. 4 line 64 – Col. 5 line 2), and a second condition (Col. 4 line 68 – Col. 5 line 2; disclosing "high" condition of switch control signal 26) allowing the first digital output portion (Out A) to correspond to the second digital input portion (B) and the second digital output

portion (Out B) to correspond to the first digital input portion (A) (Col. 4 line 64 – Col. 5 line 2); and a control arrangement (30) to switch the switching element between the first condition and the second condition (Col. 4 line 68 – Col. 5 line 2).

Regarding claim 3, wherein the control arrangement (30) has a first control input (IN A) connected with the first digital input portion (A), a second control input (IN B) connected with the second digital input portion (B), and a control output (26), the control output (26) allowing the switching element to assume the second condition (Col. 5 lines 31 – 34) if the first digital input portion is different from the second digital input portion (Col. 5 lines 44 – 46).

Regarding claim 18, wherein the switching element is a multiplexer (Fig. 6[20] disclosing multiplexing system for transmitting multiple signals A and B; See Webster Dictionary for "multiplex").

Regarding claim 19, wherein the switching element is a latched multiplexer (Fig. 6[20] disclosing multiplexing system for transmitting multiple signals by using switches 24, 24 for engaging or latching the paths between input terminals [A, B] and output terminals [Out A, Out B]).

Regarding claim 34, Fig. 6 of Adams et al. discloses a circuit comprising: a first input (A) and a second input (B); a control element (30) connected with the first input and second input; a switch (20) either switching or not switching (Col. 4 line 64 – Col. 5 line 2) the first input (A) and the second input (B) according to the control element (30); and a clocking (Clk, 38) arrangement to pipeline the switch (Col. 5 lines 18 – 20).

Regarding claim 35, wherein the first input (A) and the second input (B) are digital inputs (Col. 8 lines 5 – 6).

Regarding claim 36, wherein the control element comprises a delta-sigma modulator (Col. 6 lines 3 – 5).

Regarding claim 41, Fig. 6 of Adams et al. disclose a circuit comprising: a first input (A) and a second input (B); a control element (30) connected (IN A, INB) with the first input (A) and the second input (B); a switch (20) either switching or not switching the first input and the second input according to the control element (Col. 4 line 68 – Col. 5 line 2); and a tuning arrangement (CountA – CountB) to frequency-adjust the switch (Col. 6 lines 51 – 55).

Regarding claim 42, wherein the first input (A) and the second input (B) are digital inputs (Col. 8 lines 5 – 6).

Regarding claim 43; wherein the control element comprises a delta-sigma modulator (Col. 6 lines 3 – 5).

Regarding claim 68, Fig. 6 of Adams et al. discloses a method comprising: providing a digital input (A, B) comprising a first digital input portion (A) and a second digital input portion (B); providing a digital output comprising a first digital output portion (OUT A) and a second digital output portion (OUT B); and either switching (22, 24) the first digital input portion and the second digital input portion (Col. 4 lines 57 – 64) , to make the first digital input portion correspond with the second digital output portion (Col. 4 line 64 – Col. 5 line 2) and the second digital input portion correspond with the first digital output portion (Col. 4 line 64 – Col. 5 line 2), or not switching the first digital input portion and the second digital input

portion (Col. 4 line 64 – Col. 5 line 2), to make the first digital input portion correspond with the first digital output portion (Col. 4 line 64 – Col. 5 line 2) and the second digital input portion correspond with the second digital output portion (Col. 4 line 64 – Col. 5 line 2), wherein switching is performed when the first digital input portion and the second digital input portion are in a predetermined relationship therebetween (Col. 5 lines 44 – 46), and not switching is performed when the first digital input portion and the second digital input portion are not in the predetermined relationship therebetween (Col. 5 lines 40 – 43).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claim 44 rejected under 35 U.S.C. 103(a) as being unpatentable over Adams et al. as applied to claim 43 above, and further in view of Robertson et al. U.S. Patent No. 6,124,813

Adams et al. as applied to claim 43, fails to disclose wherein the delta-sigma modulator comprises a filtering element and a quantizer.

Fig. 1B of Robertson et al. discloses a conventional digital sigma delta modulator (Col. 6 lines 45) comprising a filter (Digital Loop Filter) and a quantizer (Digital Quantizer).

Adams et al. and Robertson et al. are common subject matter of DAC sigma-delta modulator. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to implement the Sigma-Delta modulator of Adams et al. with the filter and the quantizer taught by Robertson, because sigma delta modulator formed by filter and quantizer are conventional and well-known in the art (Robertson; Col. 6 line 45).

Allowable Subject Matter

9. Claims 2, 4 – 17, 20 – 33, 37 – 40, and 45 – 47 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

With respect to claim 2, in addition to other elements in the claim, the prior art does not teach wherein the control for switches arrangement comprises analog section.

With respect to claim 4, in addition to other elements in the claim, the prior art does not teach wherein the control arrangement comprises a subtractor, subtracting the first digital input portion from the second digital input portion, the subtractor having a subtractor output with a first subtractor output value if the first digital input portion is not in a predetermined relationship with the second digital input portion and a second subtractor output value if the first digital input portion is in a predetermined relationship with the second digital input portion.

With respect to claim 37, is object to because antecedent basis correction is required from above, and objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, in addition to other elements in the claim, the prior art does not teach wherein the clocking arrangement clocks the filter element and the quantizer.

With respect to claim 45, in addition to other elements in the claim, the prior art does not teach wherein the filter element having at least one delay element.

With respect to claim 47, in addition to other elements in the claim, the prior art does not teach, wherein the filtering element having a plurality of transconductors, and wherein the tuning arrangement frequency adjusts at least one transconductor.

Claim 69 is object to because minor correction is required from above, and would be allowable after appropriated correction in response to this office action. The prior art does not teach a first DAC having a first DAC input and a first DAC output; providing a second DAC having a second DAC input and a second DAC output; connecting the first circuit output with the first DAC input and the second circuit output with the second DAC input; subtracting the second DAC output from the first DAC output to provide a difference output; and inputting the difference output to a spectrum analyzer.

10. Claims 48 – 52, and 53 – 67 are allowed.

The following is an examiner's statement of reasons for allowance:

With respect to claims 48 and 53, in addition to other elements in the respective claim, the prior art does not teach a control element to control switching of the switch, the control element connected with the evaluation element and the switching element, the control element comprising a quantizer having a quantizer output, wherein switching between the first digital input and the second digital input depends on the quantizer output when the first digital input and the second digital input are in predetermined relationship therebetween and switching between the first digital input and the second digital input does not depend on the quantizer output when the first digital input and the second digital input are not in the predetermined relationship therebetween.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Cited References

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The cited references are relating to mismatching noise shape Digital to Analog Converter.

Contact Information

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh Van Nguyen whose telephone number is

(571) 272-1810. The examiner can normally be reached from 8:30 – 5:00 Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Michael Tokar can be reached at (571) 272-1812. The fax phone numbers for the organization where this application or proceeding is assigned are (703-872-9306) for regular communications and (703-872-9306) for After Final communications.

12/29/2004

Linh Van Nguyen

Art Unit 2819